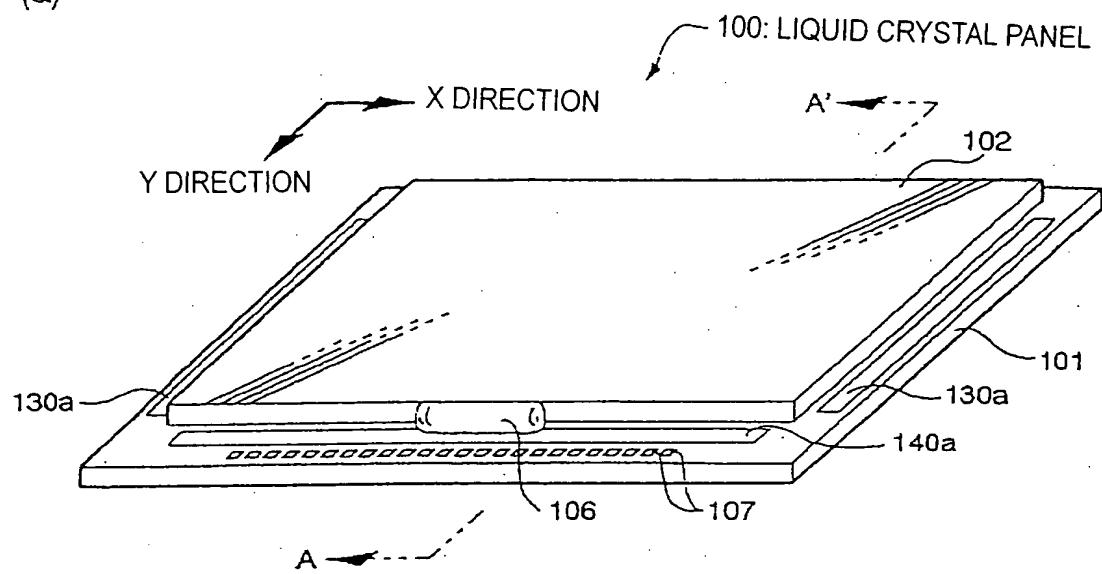


FIG. 1

(a)



(b)

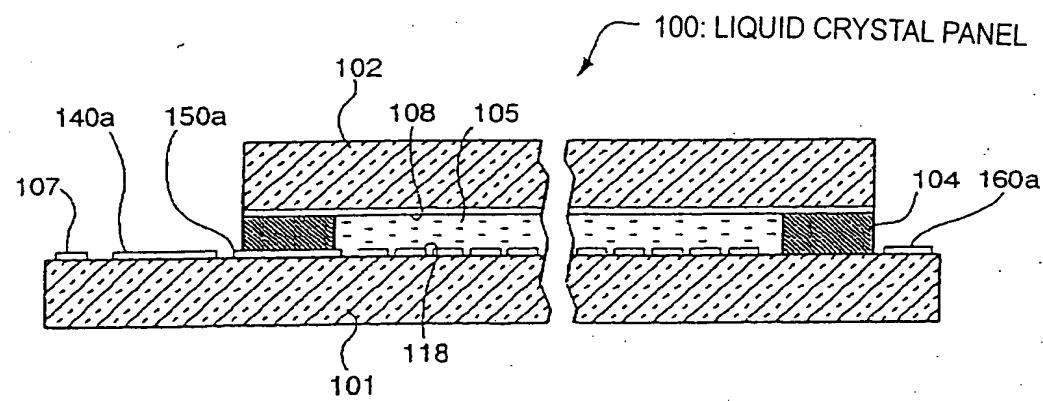


FIG. 2

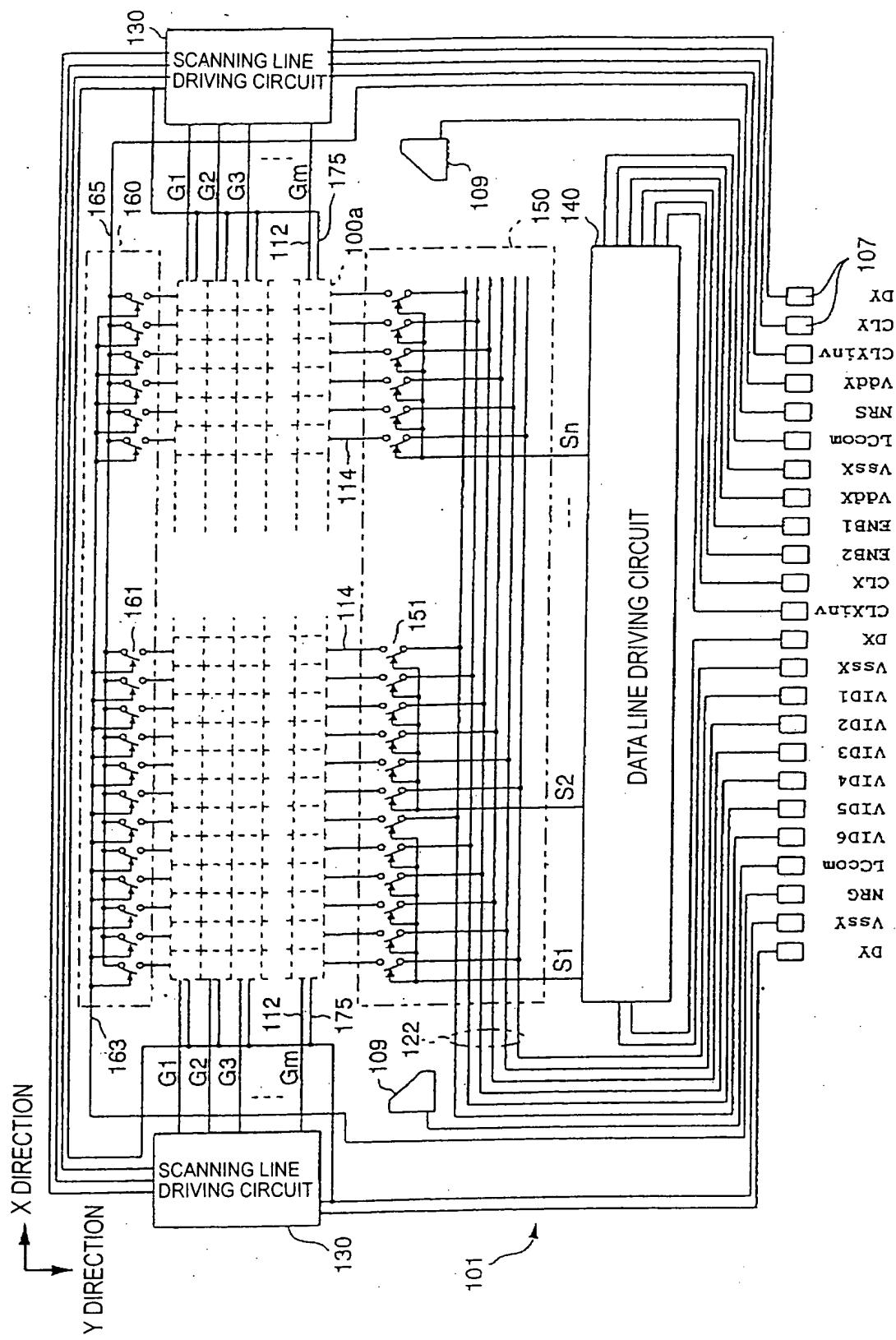


FIG. 3

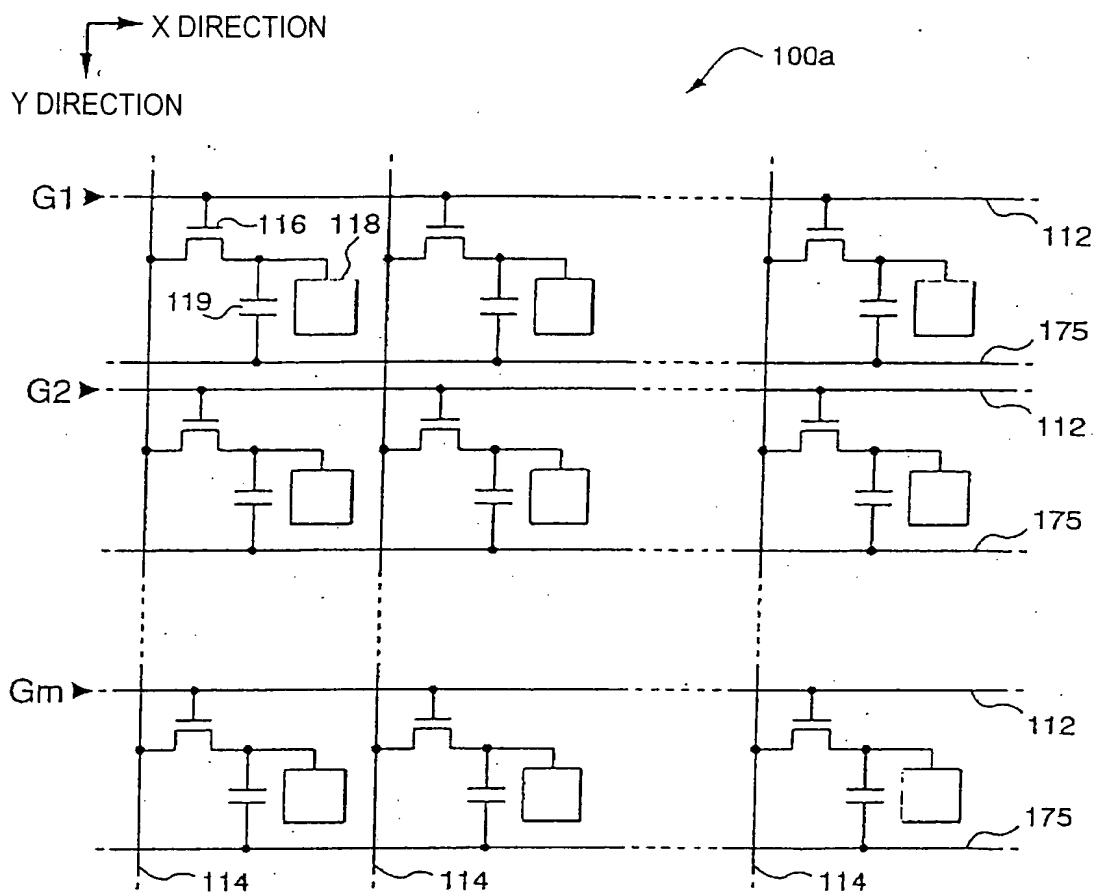


FIG. 4

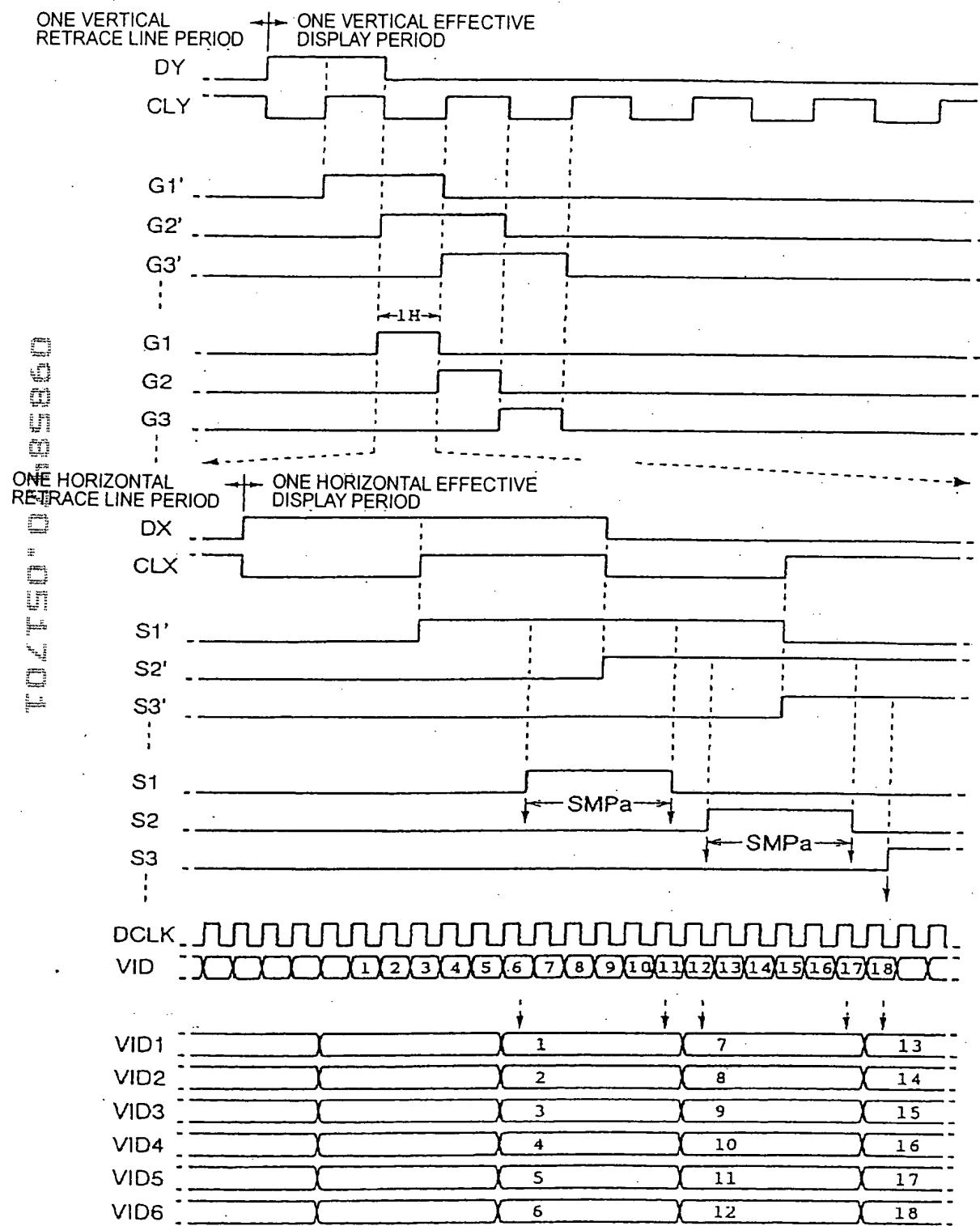


FIG. 5

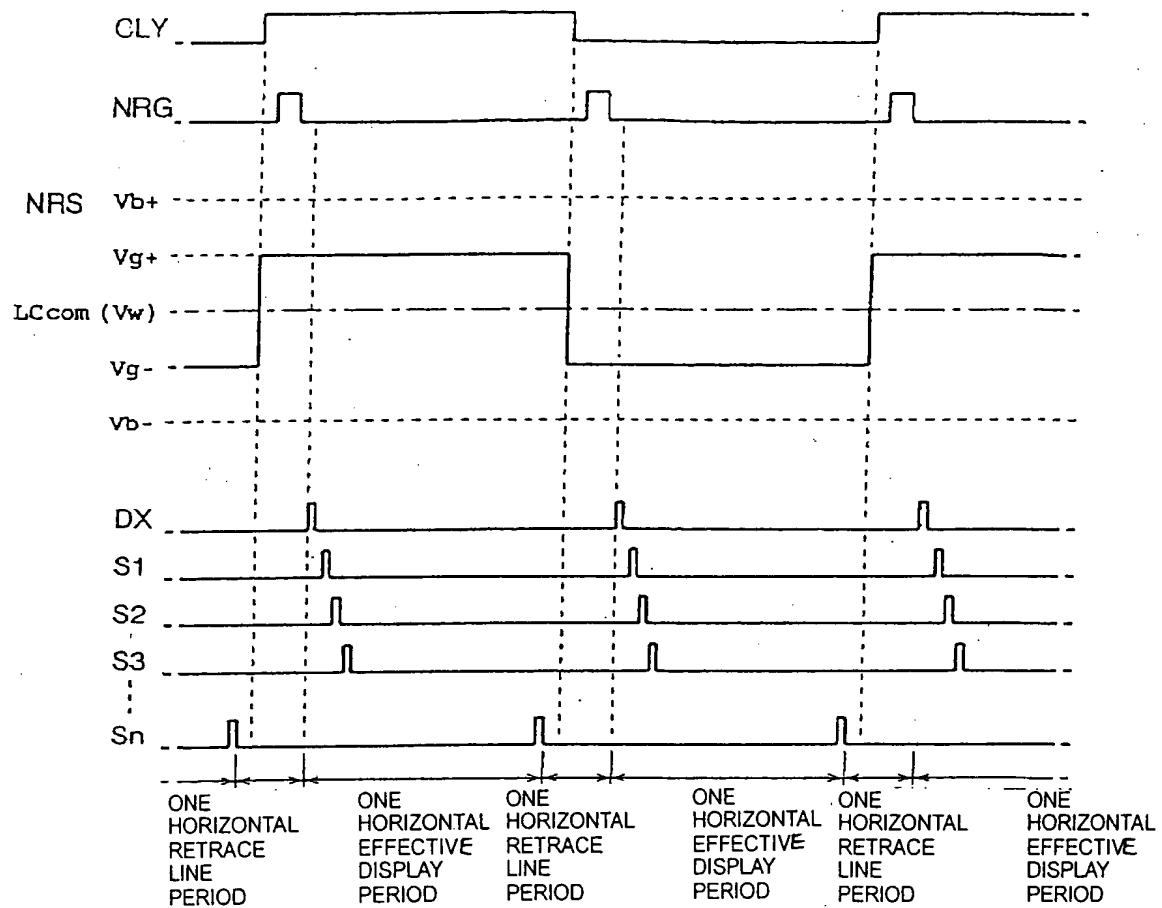


FIG. 6

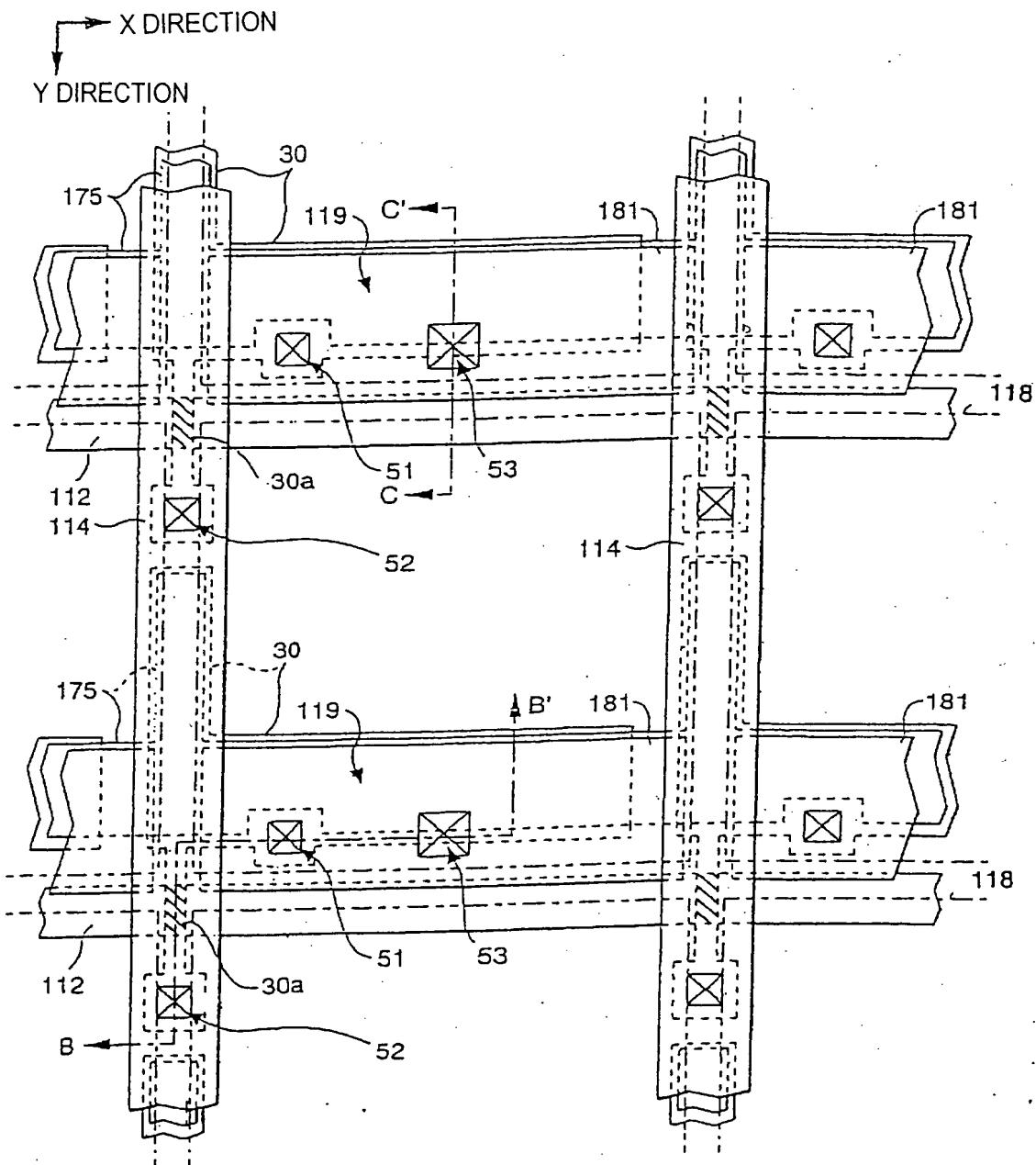
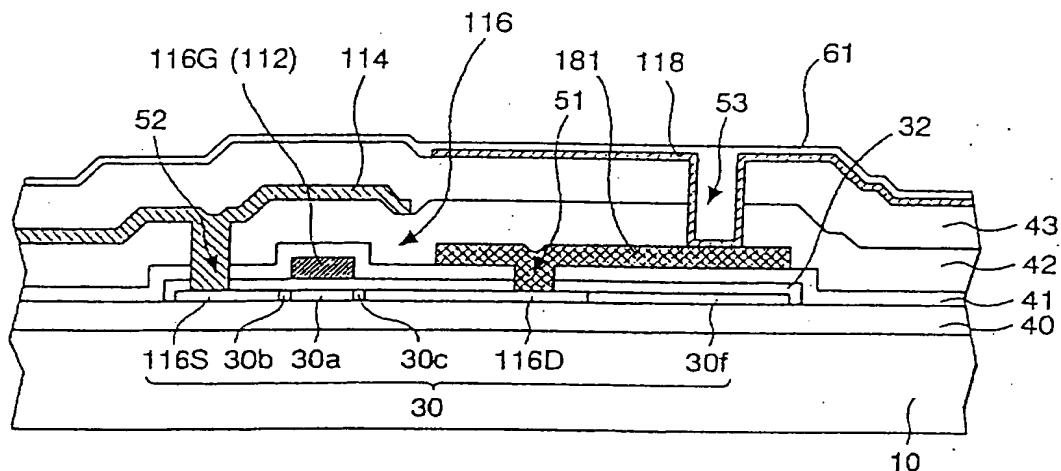
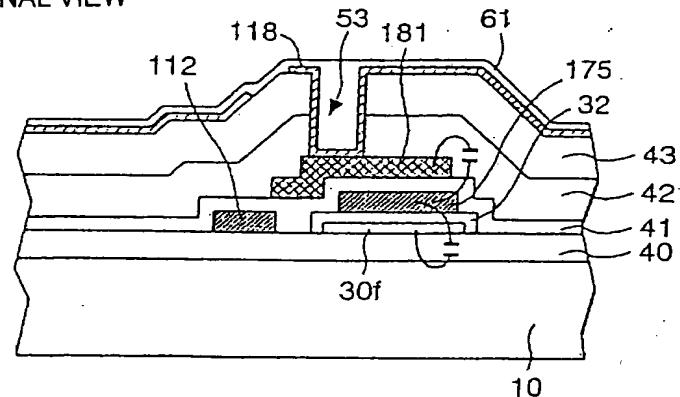


FIG. 7

(a) LINE B-B' CROSS-SECTIONAL VIEW



(b) LINE C-C' CROSS-SECTIONAL VIEW



(c) EQUIVALENT CIRCUIT OF STORAGE CAPACITOR

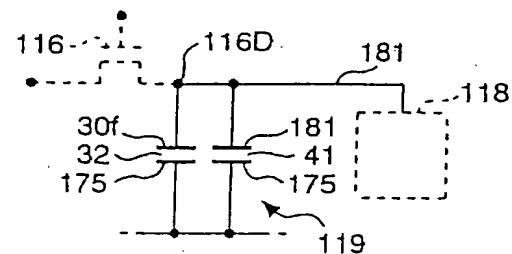


FIG. 8

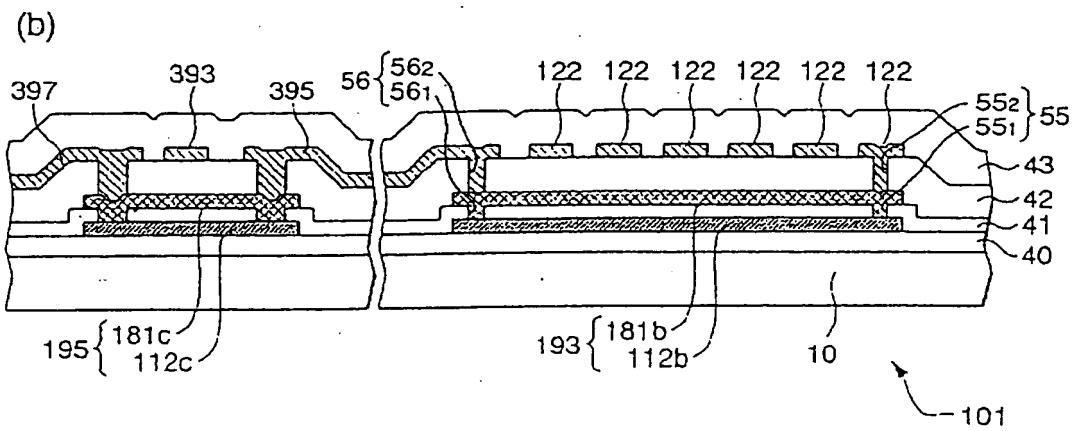
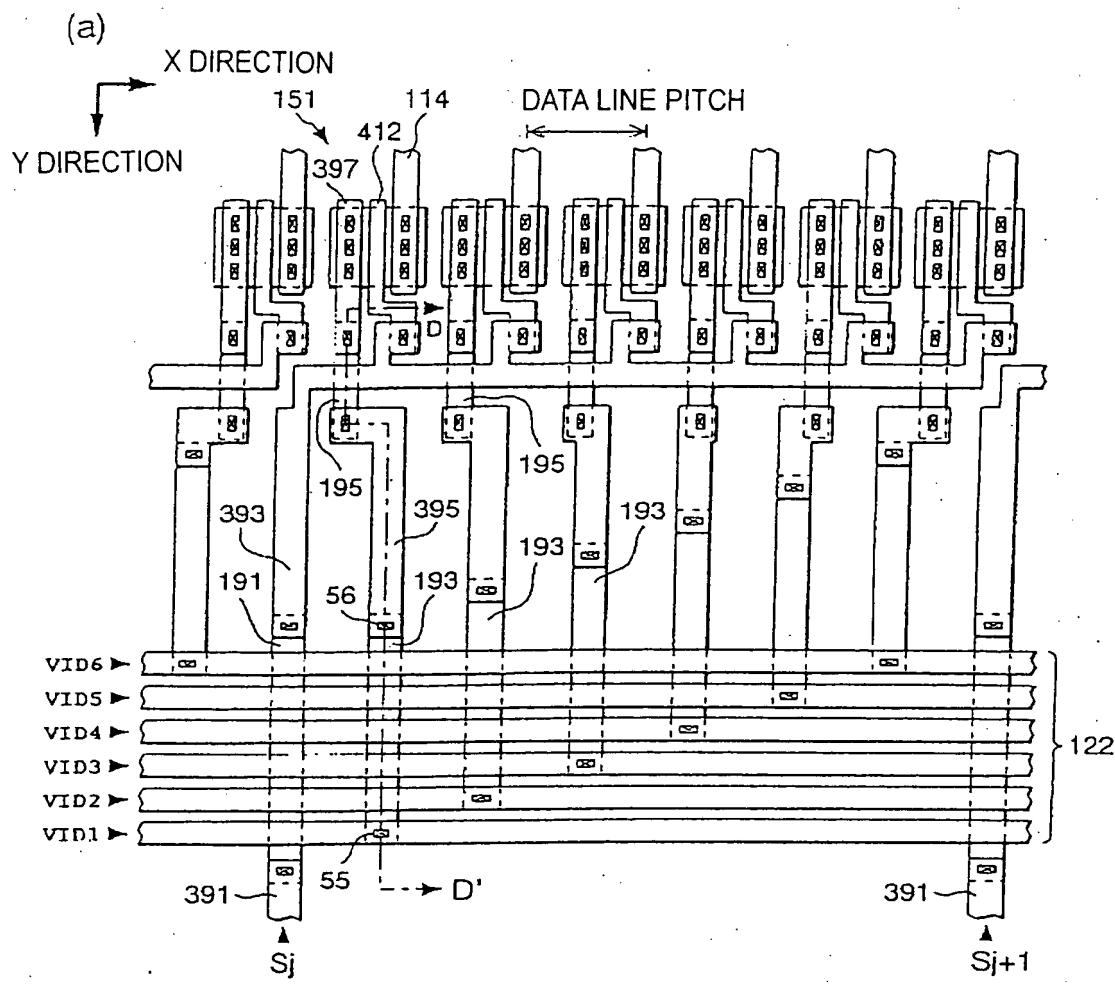
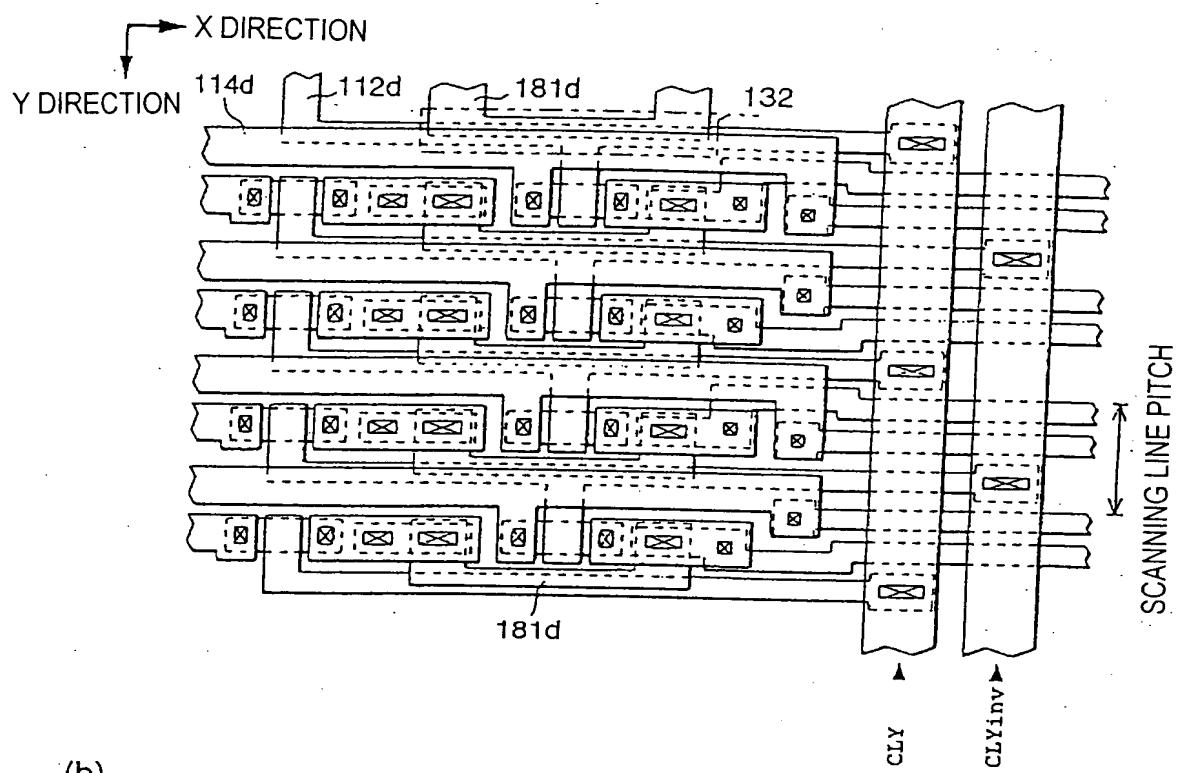


FIG. 9

(a)



(b)

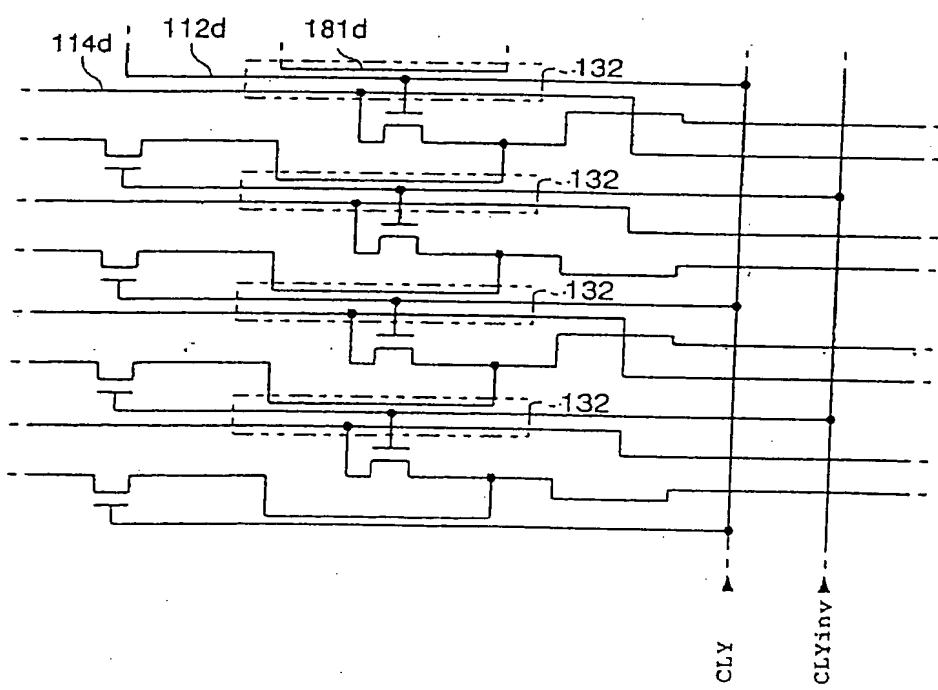
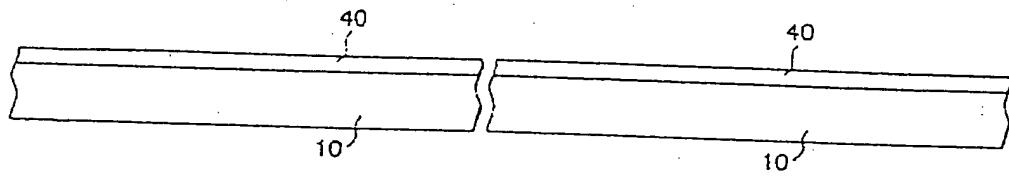


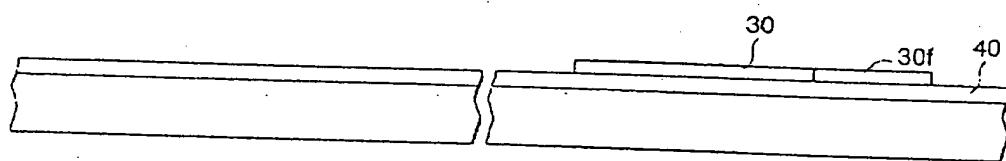
FIG. 10 |

(1)

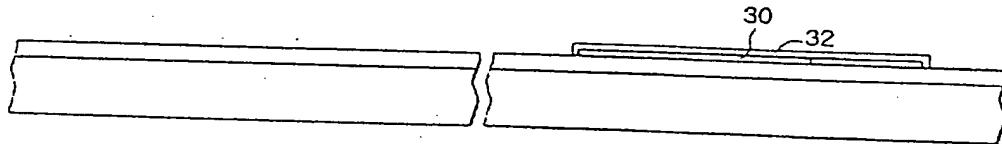
PERIPHERAL CIRCUIT REGION      DISPLAY REGION



(2)



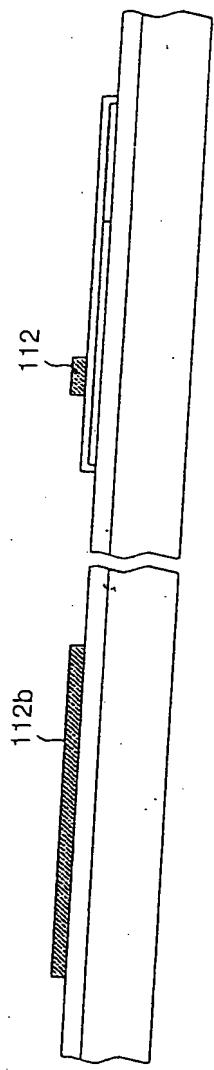
(3)



TOP SECRET // DIA//NSA//CIA

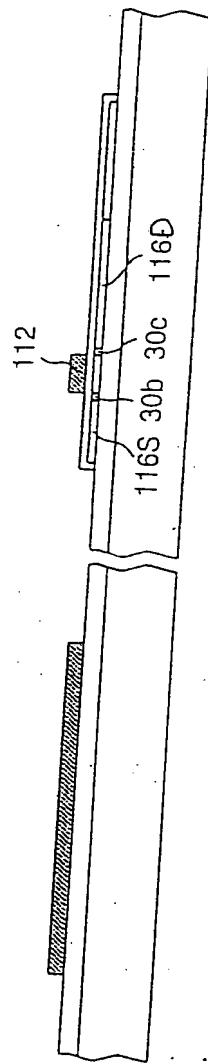
FIG. 11

FIG. 11 "DRAFTSHEET



(4)

(5)



(6)

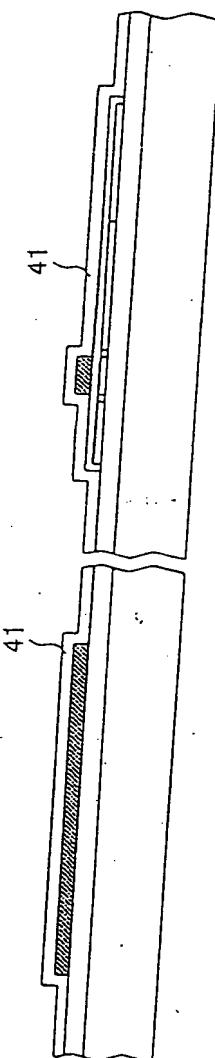
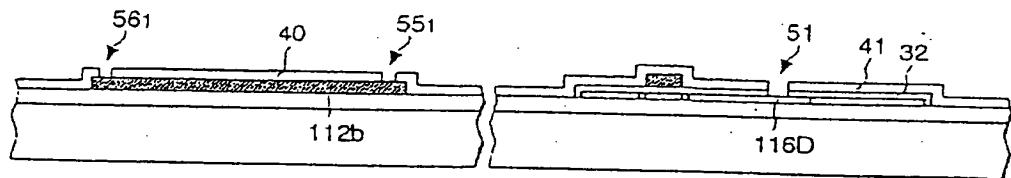
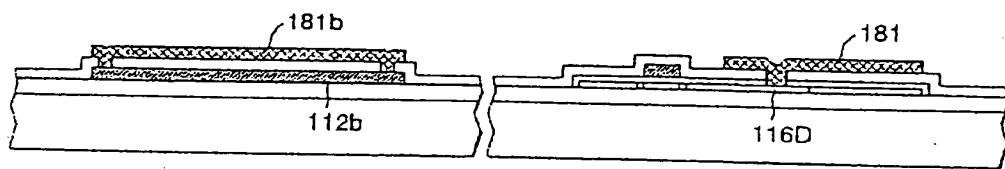


FIG. 12

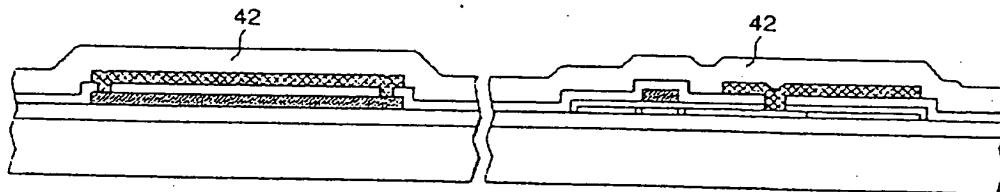
(7)



(8)



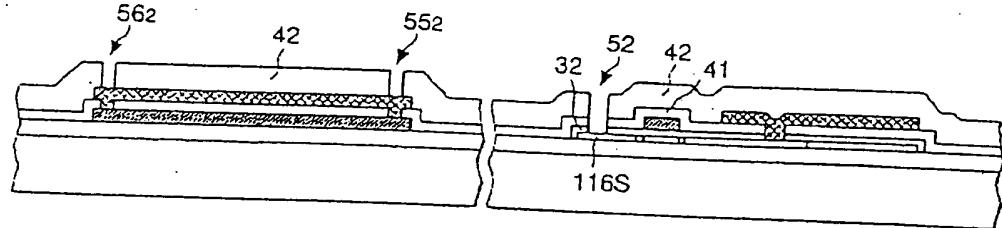
(9)



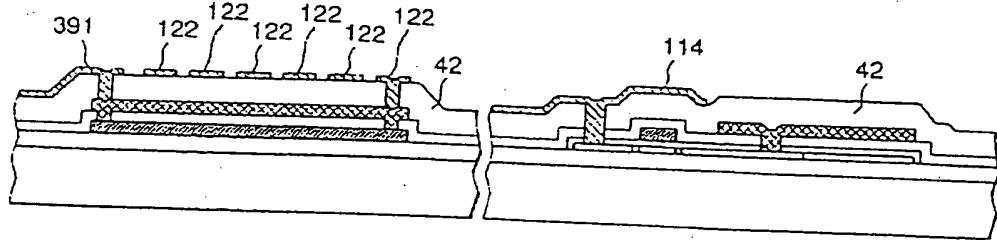
1024750 0240859260

FIG. 13

(10)



(11)



(12)

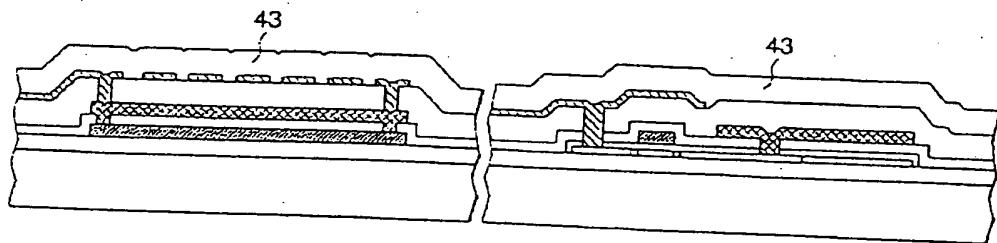
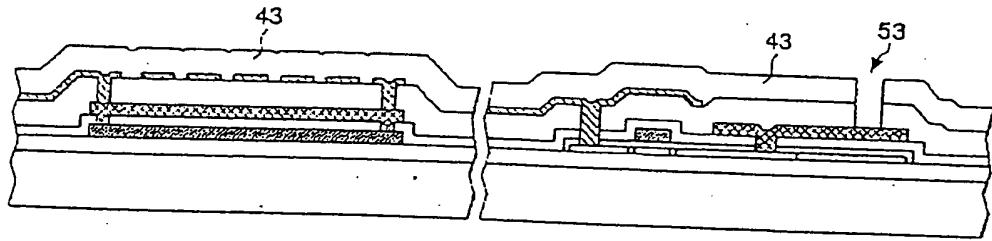


FIG. 14

(13)



(14)

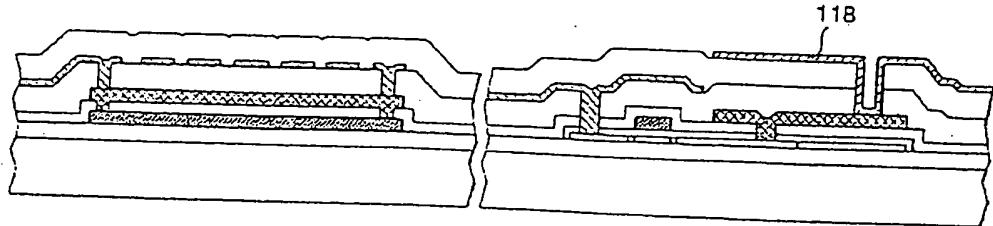
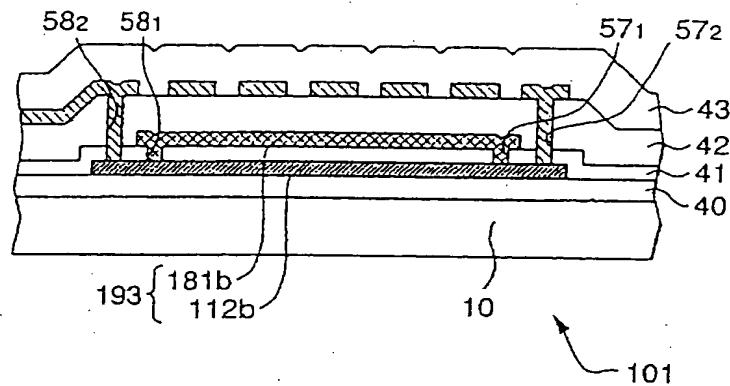


FIG. 15

(a)



(b)

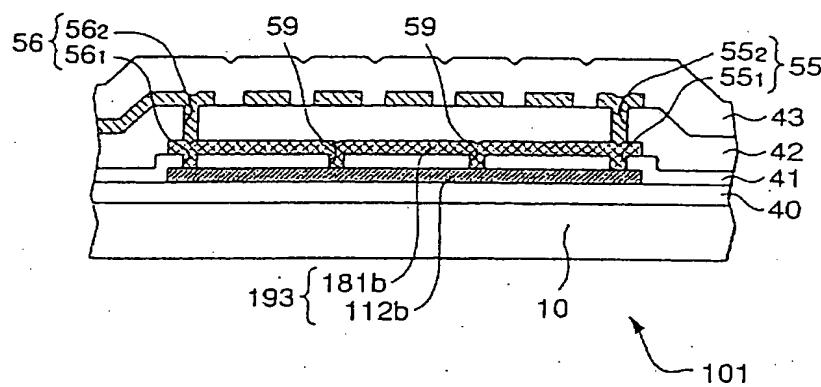


FIG. 16

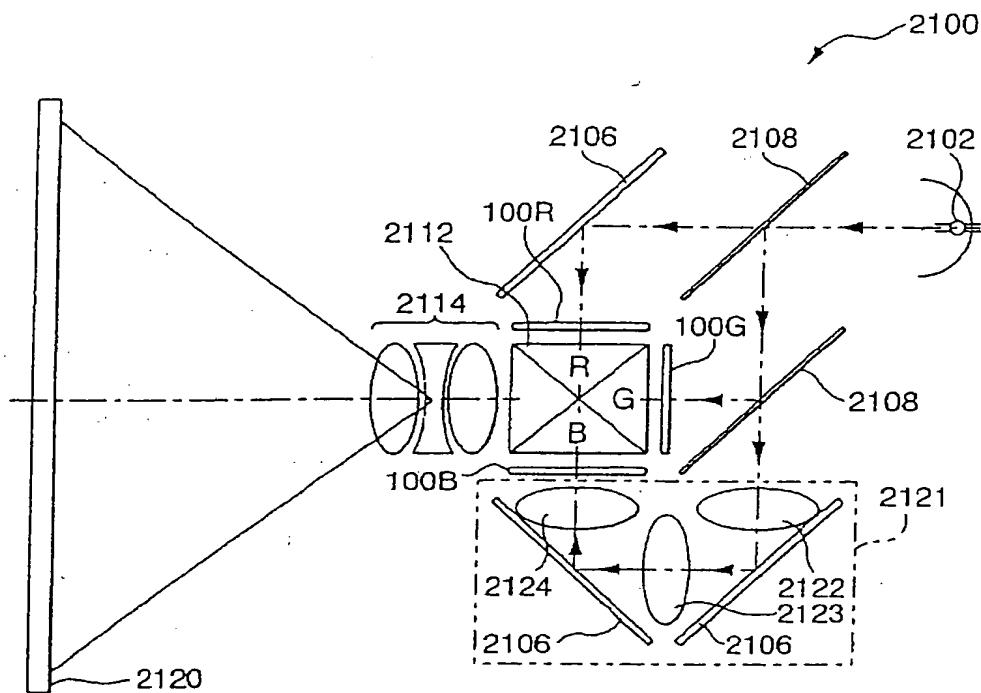


FIG. 17

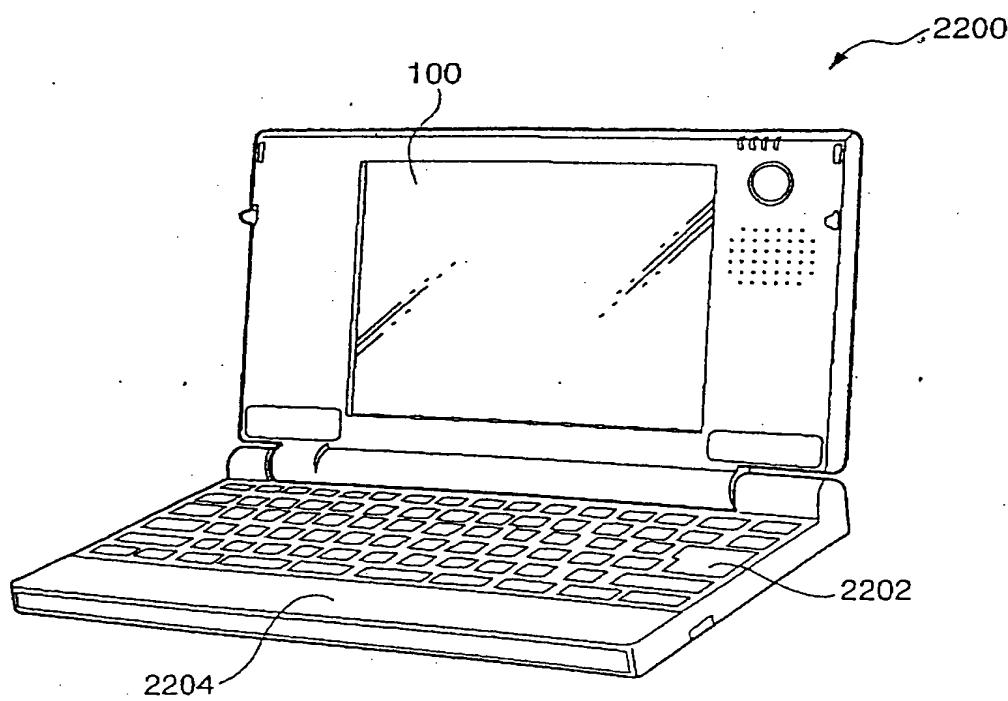


FIG. 18

